Harish Vijayakumar

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Education

Georgia Institute of Technology | Atlanta, GA
Bachelor of Science in Computer Engineering *Expected Graduation, May 2028*
GPA 3.73/4.0
Relevant Coursework: Digital System Design, Circuit Analysis, Programming HW/SW Systems, Data Struct and Algorithms

Skills

Languages: SystemVerilog, Verilog, VHDL, C, Java, Python, MATLAB
Digital Design: RTL Design, Finite State Machines, Computer Architecture, FPGA Desi
Verification: ModelSim, Cadence Xcelium, RTL Simulations, Waveform Debugging
Tools: Intel Quartus Prime, Cadence Innovus, Git, VS Code, Linux
Hardware: Intel DE10-Lite FPGA, Arduino, Oscilloscopes, Logic Analyzer
Certifications: OSHA, CITI Human Subject Research
Organizations: SiliconJackets, GT Boxing Club (Secretary), Beta Chi Theta National Fraternity
Languages: English (fluent), Tamil (fluent), Spanish (beginner)

Projects

FPGA UART Communication & DSP Platform *May 2026 - June 2026*

- Designed and implemented a modular UART communication platform featuring UART TX/RX modules, FIFO buffering, command parsing, and FSM controller, supporting 115200 baud.
- Developed a DSP subsystem which includes a moving average filter, modifiable clock divider, and seven-segment display driver for FPGA visualization.
- Verified RTL functionality using simulation and validated UART communication by connecting DE10Lite with CP2102 USB-to-UART interface and testing using Arduino IDE.

8-Bit CPU *June 2026 - July 2026*

- Created an 8-bit processor datapath consisting of a program counter, instruction memory, instruction decoder, register file, arithmetic logic unit (ALU), and FSM controller with 4 general-purpose registers.
- Implemented five logic instructions (ADD, SUB, AND, OR, XOR) with register writeback and instruction execution.
- Verified RTL components using testbenches and processor functionality on DE10-LITE hardware.

Digital Calculator Chip Design *January 2026 - March 2026*

- Implemented SystemVerilog logic for a 64-bit arithmetic calculator combining upper and lower 32-bit operations.
- Verified and synthesized the design using Xcelium, SimVision, and Innovus, achieving 99% coverage and validating SRAM behaviors.

Experience

Cultivate Lab | Athens, GA *January 2025 - January 2026*
Undergraduate Researcher

- Co-authored 2 peer-reviewed engineering education publications (FIE 2025 AND ASEE 2026) examining university student mental health and coping strategies.
- Screened 5,000+ peer-reviewed articles using Rayyan to extract and synthesize data from 35 qualifying studies.
- Held student interviews and identified relationships between reference-sheet usage and academic retention.

Office for Student Success and Achievement | Athens, GA *August 2025 - December 2025*
Peer Learning Assistant

- Led weekly problem-solving sessions for 50+ ECE students, reinforcing core circuit and systems concepts.
- Collaborated with faculty to improve lab and course materials, improving the quality of education for each class.